CLAIMS

What is claimed is:

1. A customizable development and demonstration platform for structured ASICs, comprising:

a structured ASIC built on a slice, including a programmable processor and a plurality of high speed SERDES ports; and

a FPGA communicatively coupled to said structured ASIC;

wherein one of said a plurality of high speed SERDES ports is driven by a test block in said structured ASIC to run signal integrity tests.

2. The platform of claim 1, wherein at least one of said a plurality of high speed SERDES port is pinned out to be driven by said FPGA.

3. The platform of claim 2, wherein said at least one of said a plurality of high speed SERDES port is driven from a link layer realized in said FPGA.

4. The platform of claim 3, wherein said platform implements at least one of SATA, GigE, XAUI, XGXS, and Fibre Channel.

5. The platform of claim 1, wherein the number of said a plurality of high speed SERDES ports is eight.

6. The platform of claim 1, wherein said a plurality of high speed SERDES ports are GigaBlaze ports.

7. The platform of claim 1, wherein a second port of said a plurality of high speed

SERDES ports is connected to a direct memory device in said structured ASIC for allowing flexible pattern transmission.

8. The platform of claim 1, wherein said FPGA is used to implement a PCI Express interface to develop a PCI Express endpoint vehicle.

9. The platform of claim 1, wherein said FPGA is used to implement special function customer logic to prove a concept.

10. The platform of claim 9, wherein said special function customer logic is encryption co-processor logic in said FPGA to secure communications between Ethernet ports on a customer ASIC.

11. The platform of claim 1, wherein said programmable processor is an ARM processor.

12. The platform of claim 1, wherein when said platform is for demonstration use, distribution software in the form of open source RTOS and router applications are ported to said platform.

13. The platform of claim 1, wherein said structured ASIC further comprises at least one of low speed serial interface and 10/100 Ethernet port, through which external I/Os are supported.

14. The platform of claim 1, wherein said test block is used to show electrical characteristics of intellectual property of said a plurality of high speed SERDES ports.

15. The platform of claim 1, wherein said structured ASIC is a RapidChip™ and said slice is a RapidSlice™.

16. A customizable development and demonstration platform for structured ASICs, comprising:

a structured ASIC built on a slice, including a programmable processor and a plurality of high speed SERDES ports,

wherein one of said a plurality of high speed SERDES ports is driven by a test block in said structured ASIC to run signal integrity tests.

17. The platform of claim 16, wherein said platform is a router/switch demonstration vehicle.

18. The platform of claim 16, wherein switch application software is modified to implement one of a customer switch, a load balancer and a firewall.

19. The platform of claim 16, wherein said structured ASIC is a RapidChip™ and said slice is a RapidSlice™.

20. A customizable development and demonstration platform for structured ASICs, comprising:

a structured ASIC built on a slice, including a programmable processor and a plurality of high speed SERDES ports; and

a FPGA communicatively coupled to said structured ASIC;

wherein one of said a plurality of high speed SERDES ports is driven by a test block in said structured ASIC to run signal integrity tests and to show electrical characteristics of intellectual property of said a plurality of high speed SERDES ports, and at least one of said a plurality of high speed SERDES port is pinned out to be driven from a link layer realized in said FPGA.

21. The platform of claim 20, wherein said platform implements at least one of SATA, GigE, XAUI, XGXS, and Fibre Channel.

22. The platform of claim 20, wherein the number of said a plurality of high speed SERDES ports is eight.

23. The platform of claim 20, wherein said a plurality of high speed SERDES ports are GigaBlaze ports.

24. The platform of claim 20, wherein a second port of said a plurality of high speed SERDES ports is connected to a direct memory device in said structured ASIC for allowing flexible pattern transmission.

25. The platform of claim 20, wherein said FPGA is used to implement a PCI Express interface to develop a PCI Express endpoint vehicle.

26. The platform of claim 20, wherein said FPGA is used to implement special function customer logic to prove a concept.

27. The platform of claim 26, wherein said special function customer logic is encryption co-processor logic in said FPGA to secure communications between Ethernet ports on a customer ASIC.

28. The platform of claim 20, wherein said programmable processor is an ARM processor.

29. The platform of claim 20, wherein when said platform is for demonstration use, distribution software in the form of open source RTOS and router applications are ported to said platform.

30. The platform of claim 20, wherein said structured ASIC further comprises at least one of low speed serial interface and 10/100 Ethernet port, through which external I/Os are supported.

31. The platform of claim 20, wherein said structured ASIC is a RapidChip™ and said slice is a RapidSlice™.